CLAIMS

What is claimed is:

1. A method of fabricating a double gate MOSFET device, comprising:

providing a silicon on insulator (SOI) substrate with a silicon layer overlying an insulating layer;

forming a cap oxide layer on said silicon on insulator (SOI) substrate;

providing a photoresistor layer with a pattern defining source, drain and channel regions on said cap oxide layer;

etching said cap oxide layer to form a hard mask;

removing said photoresistor layer;

etching said silicon layer using the hard mask of said cap oxide layer as an etching mask to form the source, drain and channel regions extending from said insulating layer, said channel being a fin structure with a top surface and two opposing sidewalls, and form a recess in said insulating layer under each said opposing sidewall of said fin structure;

forming a gate dielectric layer along each said opposing sidewall;

forming a conductive gate layer straddling said fin structures; and

performing a first titled ion implantation to implant dopants in said conductive gate layer, thereby said conductive gate layer having a first conductivity.

2. The method of claim 1, wherein further comprising a step of thinning down said silicon layer by forming a thermal oxide layer

through thermal oxidation prior to forming said cap oxide layer on said silicon on insulator (SOI) substrate.

3. The method of claim 2, further comprising removing said thermal oxide layer with a buffered oxide etch (BOE) prior to forming said cap oxide layer on said silicon on insulator (SOI) substrate.

4. The method of claim 1, wherein said step of etching said silicon layer comprising a step of performing a reactive ion etching process using the hard mask of said cap oxide layer as the etching mask.

5. The method of claim 4, wherein said step of etching said silicon layer further comprising a step of performing wet etching following said reactive ion etching process.

6. The method of claim 1, wherein said insulating layer of said silicon on insulator (SOI) substrate comprises a buried oxide layer.

7. The method of claim 1, wherein the step of forming said gate dielectric layer comprises forming a silicon dioxide spacer by in-situ steam generation (ISSG) process.

8. The method of claim 1, wherein further comprising a step of performing a second titled ion implantation to implant dopants in said fin structures following the step of overetching said silicon layer, thereby said fin structures having said first conductivity.

9. The method of claim 1, wherein the step of forming said

conductive gate layer comprises forming a polysilicon layer on said fin structures by a low pressure chemical vapor deposition method.

10. The method of claim 1, wherein further comprising a step of performing a rapid thermal annealing (RTA) process by reflowing for about 20 seconds at a temperature of 850℃, following the step of performing said first inclined ion implantation.

11. A method of fabricating a double gate CMOS device, comprising:

providing a silicon on insulator (SOI) substrate with a silicon layer overlying an insulating layer;

forming a cap oxide layer on said silicon on insulator (SOI) substrate;

providing a first photoresistor layer with a pattern defining source, drain and channel regions on said cap oxide layer;

etching said cap oxide layer to form a hard mask;

removing said first photoresistor layer;

etching said silicon layer using the hard mask of said cap oxide layer as an etching mask to form the source, drain and channel regions extending from said insulating layer, said channel being a fin structure with a top surface and two opposing sidewalls, and form a recess in said insulating layer under each said opposing sidewall of said fin structure;

forming a gate dielectric layer along each said opposing sidewall;

forming a conductive gate layer straddling said fin structures;

forming a second photoresistor layer with a pattern defining a first MOS device region on said conductive gate layer;

performing a first titled ion implantation to implant dopants in

said conductive gate layer of said first MOS device region, thereby said conductive gate layer having a first conductivity;

removing said second photoresistor layer;

forming a third photoresistor layer with a pattern defining a second MOS device region on said conductive gate layer;

performing a second titled ion implantation to implant dopants in said conductive gate layer of said second MOS device region, thereby said conductive gate layer having a second conductivity; and

removing said third photoresistor layer.

12. The method of claim 11, wherein prior to the step of forming said conductive gate layer on said fin structures, further comprising steps of performing a third titled ion implantation to implant dopants in said fin structures of said first MOS device region, thereby said fin structures of said first MOS device region having said first conductivity, and performing a fourth titled ion implantation to implant dopants in said fin structures of said second MOS device region, thereby said fin structures of said second MOS device region having said second conductivity.

13. The method of claim 11, wherein said step of etching said silicon layer comprising a step of performing a reactive ion etching process using the hard mask of said cap oxide layer as the etching mask.

14. The method of claim 13, wherein said step of etching said silicon layer further comprising a step of performing wet etching following said reactive ion etching process.

15. The method of claim 11, wherein said insulating layer of said silicon on insulator (SOI) substrate comprises a buried oxide layer.

16. The method of claim 11, wherein the step of forming said gate dielectric layer comprises forming a silicon dioxide spacer by in-situ steam generation (ISSG) process.

17. A double gate FinFET transistor device, comprising:

a semiconductor substrate;

a buried oxide layer on said semiconductor substrate;

a double gate FinFET transistor standing on said buried oxide layer, said double gate FinFET transistor including a channel being a fin structure with a top surface and two opposing sidewalls and having a recess under each said opposing sidewall of said channel in said buried oxide layer and a spacer along said two opposing sidewalls, a double gate straddling said channel and a pair of source/drain islands respectively linking either side of said channel on said buried oxide layer perpendicularly to said double gate.

18. A double gate FinFET transistor device of claim 17, wherein said channel includes a silicon fin.

19. The double gate FinFET transistor device of claim 17, wherein further comprises a cap oxide layer on said top surface of said fin structure and said source/drain regions.

20. The double gate FinFET transistor device of claim 17, wherein said double gate includes doped polysilicon.